Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of clearing data in a memory of a computer system, the computer system comprising a processor, and a memory controller electrically connected to the processor and the memory for controlling accessing operations of the memory, the memory comprising a plurality of memory units, the method comprising:

the processor generating a predetermined logic value, and delivering the predetermined logic value to the memory controller; and

the memory controller ~~repeatedly~~ consecutively overwriting data stored in the plurality of memory units by the predetermined logic value;

wherein if the plurality of memory units have discontinuous addresses, a memory address table is provided to the memory controller for writing the predetermined logic value to the plurality of memory units, the memory address table comprising a plurality of fields, each field including a physical memory address, a bit length, and a flag for respectively recording a start address, a bit length, and indicating whether data is an end portion.

Claim 2 (Original): The method of claim 1 wherein if the plurality of memory units have continuous addresses, a source memory address and a

bit length are delivered to the memory controller.

Claims 3-4 (Cancelled)

Claim 5 (Original): The method of claim 1 wherein the predetermined logic value is "0" or "1".

Claim 6 (Currently Amended): A computer system comprising:

a processor for controlling operations of the computer system;

a memory including a plurality of memory units for storing data; and

a memory controller electrically connected to the processor and the memory, the memory controller comprising:

an address register for storing a plurality of memory addresses corresponding to the plurality of memory units;

a data register; and

a data clear module for transmitting a predetermined logic value generated by the processor to the data register so that the predetermined logic value consecutively overwrites data stored in the plurality of memory units one by one;

wherein if the plurality of memory units have discontinuous addresses, a memory address table is provided to the memory controller for writing the predetermined logic value to the plurality of memory units, the memory address table comprising a plurality of fields, each field including a physical memory address, a bit length, and a flag for respectively recording a start address, a bit length, and indicating whether data is an end portion.

Claim 7 (Original): The computer system of claim 6 wherein if the plurality

of memory units have continuous addresses, the data clear module will generate a plurality of memory addresses according to a source memory address and a bit length, and deliver the plurality of memory addresses to the address register so as to write the predetermined logic value to the memory units corresponding to the plurality of memory addresses.

Claim 8 (Currently Amended): The computer system of claim 6 wherein if the plurality of memory units have discontinuous addresses, the data clear module utilizes [[a]] the memory address table for generating a plurality of memory addresses to the address register, and writes the predetermined logic value to the plurality of memory units corresponding to the plurality of memory addresses.

Claim 9 (Original): The computer system of claim 8 wherein the memory address table is generated by an operating system of the computer system.

Claim 10 (Original): The computer system of claim 6 wherein the memory controller is installed in a north bridge circuit.

Claim 11 (Original): The computer system of claim 10 wherein the north bridge circuit further comprises a display controller to generate image signals for driving a display device of the computer system.

Claim 12 (Original): The computer system of claim 11 wherein the memory comprises a display memory for storing operation data of the display controller, and a system memory for storing operation data of the

processor.

Claim 13 (Original): The computer system of claim 12 wherein the plurality of memory units are located in the display memory or in the system memory.